Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-19. (Cancelled)

20. (Currently Amended) An unpredictable microprocessor or microcomputer comprising:

three distinct locations each for receiving memory;

in a first location, a main memory including an operating system, a main program, and a secondary program, wherein said secondary program is not related to the main program;

in a second location, a first RAM-type working memory;

in a third location, a second RAM-type working memory;

a processor adapted to execute instructions from one or more of said main memory, said first working memory and said second working memory;

a bus connecting the processor to the main memory, the first working memory and the second working memory;

switching means for making said processor unpredictable, said switching means unpredictably jumping, while the programs are running, from one of the two working memories to the other working memory while saving the contents of the two working memories, said switching means comprising:

access registers associated with each of the main memory, the first working

memory and the second working memory;

at least one first block of registers that stores the operating context of the programs in the main memory; and

a switching circuit that enables one of the working memories and controls the access registers associated with each of the main memory, the first working memory and the second working memory.

21. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, further comprising a second block of registers for storing the operating context of the secondary program.

22. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, further including means for de-correlating the running of the programs from an isochronous clock.

23. (Previously Presented) The microprocessor or microcomputer according to claim 21, wherein the main program can enable or inhibit the switching means by loading the switching circuit to switch and enable the working memories and the first block and second block of storage registers associated with each respective working memory, and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program.

24. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, wherein the second working memory and its access registers are substituted for the first working memory and its access registers in utilization by the main program.

25. (Currently Amended) The unpredictable microprocessor or microcomputer according to claim 22, wherein the de-correlating means comprise a random number generator for triggering, via an interrupt circuit, ~~the~~ a random interrupt for desynchronizing the running of the programs in the processor, by unpredictably jumping to the secondary program.

26. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 23, further including means for de-correlating the running of the programs from an isochronous clock, wherein the de-correlating means comprises a time counting system independent from the processor that, after the time count, triggers an interrupt for returning from the secondary program to the main program.

27. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 23, further including means for de-correlating the running of the programs from an isochronous clock, wherein the switching means is controlled by the processor and its program, by the de-correlating means, by a timer, or by any combination of at least two of the three named elements.

28. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, wherein the switching means is enabled by being loaded by the processor running a sequence in the main program.

29. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, wherein the secondary program uses a working space identical to that of the main program in the main memory.

30. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, wherein the secondary program uses a working space smaller than that of the main program.

31. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, wherein the switching means carry out the substitution of the memories and the associated contexts within the execution cycle of an instruction from the microprocessor.

32. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, wherein the secondary program does not modify the general operating context of the main program in order to allow the main program to return without having to reestablish said context.

33. (Currently Amended) The unpredictable microprocessor or microcomputer according to claim ~~32~~ 20, wherein the context of the main program is reestablished either automatically by the secondary program or automatically by the switching means before returning control to the main program.

34. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, further comprising means for substituting the memory of the secondary program for the memory of the main program.

35. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 20, wherein the main program can use the first working memory and the second working memory alternately or simultaneously.

36. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 23, wherein loading of the switching circuit makes it possible to mask or unmask de-correlating interrupts.

37. (Previously Presented) The unpredictable microprocessor or microcomputer, according to claim 25, wherein an interrupt triggered by the secondary program effects return to the main program after the switching register has been properly loaded, by executing an instruction of the main program or the secondary program, in order to unmask the interrupts.

38. (Previously Presented) The unpredictable microprocessor or microcomputer, according to claim 20, wherein the microprocessor or microcomputer is embodied in a monolithic integrated circuit.

39. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 21, further including means of de-correlating the run-through of the programs with respect to an isochronal clock.

40. (Cancelled)

41. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 21, wherein the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by a main program, with said first memory and the associated access registers of the first memory.

42. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 22, wherein the de-correlating means comprise a random generator.

43. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 25, wherein the de-correlation means include a time counting system independent of the processor for enabling, at the end of a time count, an interruption trigger to return from the secondary program to the main program.

44. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 25, wherein the switching means is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or a combination of at least two out of the three named elements.

45. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 22, wherein the main program is adapted to enable or inhibit the switching means by loading the switching circuit of working memories and of the memorization register blocks associated with each respective working memory.

46. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 22, wherein the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by the main program, with said first working memory and the associated access registers of the first working memory.

47. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 26, wherein the switching means is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or by a combination of at least two out of the three named elements.

48. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 25, wherein the interrupt circuit triggers the random number generator

to thereby trigger the random interrupt to desynchronize execution of the programs in the processor, by random connection to the secondary program.

49. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 26, wherein the de-correlation means include a time counting system independent of the processor for enabling, at the end of a time count, the triggering of the random interrupt to return from the secondary program to the main program, and the switching means is controlled by one of the microprocessors and the program thereof, the random interruption system, a time counter or by a combination of at least two of the three named elements.

50. (Previously Presented) The unpredictable microprocessor or microcomputer according to claim 21, wherein the switching means is confirmed by loading from the processor executing a main program sequence.